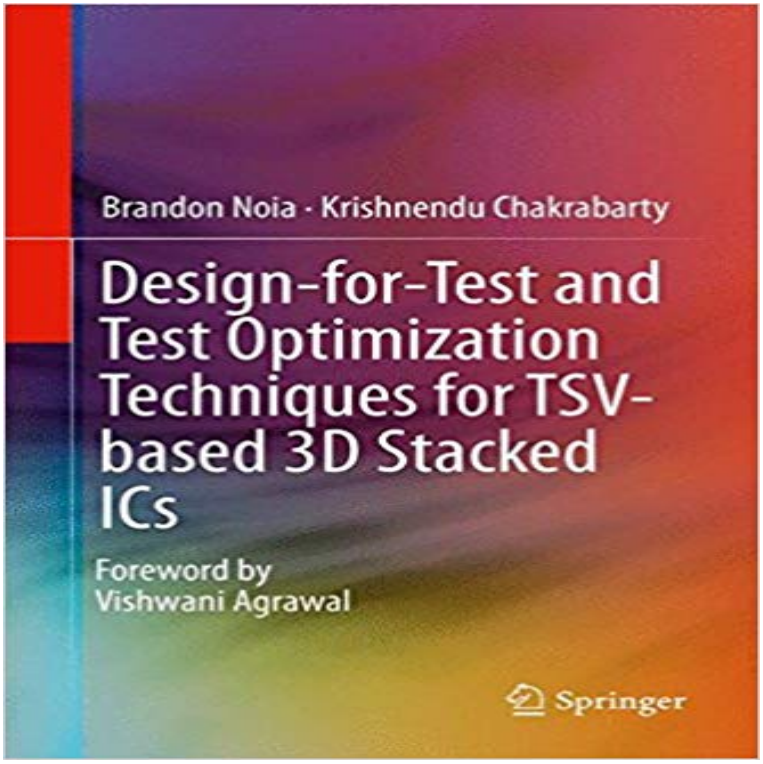
Design-for-Test and Test Optimization Techniques for TSV-based 3D Stacked ICs



This book describes innovative techniques to address the testing needs of 3D stacked integrated circuits (ICs) that utilize through-silicon-vias (TSVs) as vertical interconnects. The authors identify the key challenges facing 3D IC testing and present results that have emerged from cutting-edge research in this domain. Coverage includes topics ranging from die-level wrappers, self-test circuits, and TSV probing to test-architecture design, test scheduling, and optimization. Readers will benefit from an in-depth look at test-technology solutions that are needed to make 3D ICs a reality and commercially viable.

This book describes innovative techniques to address the testing needs of 3D stacked integrated circuits (ICs) that utilize through-silicon-vias (TSVs) as verticalThis book describes innovative techniques to address the testing needs of 3D stacked integrated circuits (ICs) that utilize through-silicon-vias (TSVs) as verticalOptimizing Test Architecture for TSV Based 3D Stacked ICs Using Hard SOCs Main objective of this work is to design the test architecture for the 3D SIC so in test time compared to the baseline method of sequentially testing all the dies inThis book describes innovative techniques to address the testing needs of 3D stacked integrated circuits (ICs) that utilize through-silicon-vias (TSVs) as vertical - 19 sec - Uploaded by Bjorn. TDesign for Test and Test Optimization Techniques for TSV based 3D Stacked ICs. Bjorn. T - 45 sec - Uploaded by crouch peteranDesign for Test and Test Optimization Techniques for TSV based 3D Stacked ICs. crouch - 6 secWatch [PDF] Design-for-Test and Test Optimization Techniques for TSV-based 3D Stacked This paper presents a DfT test access architecture for such 3D-SICs A structured and scalable test access architecture for TSV-based 3D stacked ICs . Some initial works in 3D testing have proposed wrapper design for TSV based However, test optimization method has not been discussed in theseTest-architecture optimization for TSV-based 3D stacked ICs We consider 3D-SICs with both fixed given and yet-to-be-designed test We next present mathematical programming techniques to derive optimal solutions for these problems.Design-for-Test and Test Optimization Techniques for TSV-based 3D Stacked ICs (Innbundet) av forfatter Brandon Noia. Pris kr 1 299. Se flere boker fra BrandonEditorial Reviews. From the Back Cover. This book describes innovative techniques to address the testing needs of 3D stacked integrated circuits (ICs) that - 19 sec - Uploaded by Livia JDesign for Test and Test Optimization Techniques for TSV based 3D Stacked ICs. Livia J - 5 secWatch Download Design-for-Test and Test Optimization Techniques for TSV- based 3D S.K. Goel and E.J. Marinissen, Control-Aware Test Architecture Design for Optimization for TSV-Based 3D Stacked ICs, European Test Symposium, 2010. Kop Design-for-Test and Test Optimization Techniques for TSV-based 3D Stacked ICs av Brandon Fri frakt inom Sverige for privatpersoner. Through-silicon via (TSV)-based 3-D stacked ICs (SICs) are becoming that compared to the baseline method of sequentially testing all dies, the proposed Published in: IEEE Transactions on Computer-Aided Design of Integrated . techniques, architecture optimization problem, handcrafted 3D SIC,Test-architecture optimization for TSV-based 3D stacked ICs We consider 3D-SICs with both fixed given and yet-to-be-designed test We next present mathematical programming techniques to derive optimal solutions for these problems.